

Appl. No. 09/751,427

Amdt. dated September 18, 2003

Reply to Office Action of July 16, 2003

REMARKS

This Amendment is in response to the Office Action mailed July 16, 2003. In the Office Action, the Examiner rejected claims 1-25 under 35 U.S.C. § 102. Reconsideration in light of the amendments and remarks made herein is respectfully requested.

Claim Amendments

Applicant has amended claims 6, 8, 10, 11, 13, 16, and 17 to improve the grammar.

Rejection Under 35 U.S.C. § 102

2. The Examiner rejects claims 1-25 under 35 U.S.C. § 102(e) as being anticipated by Kelly et al. (US 6,357,013).

a. As per claims 1 and 14, the Examiner asserts that Kelly discloses each and every limitation of the claims citing column 2, lines 26-40. The cited portion of Kelly discloses a transition from SLEEP mode to IDLE mode using a CPU-PCI bridge. Applicant fails to understand what it is in the cited portion of Kelly that the Examiner considers to disclose a configurable link with the claimed capabilities. Applicant respectfully requests that the Examiner elaborate on how Kelly discloses the apparatus claimed if the Examiner intends to sustain this rejection.

b. As per claim 2, applicant relies on the patentability of the claim from which this claim depends to traverse the rejection without prejudice to any further basis for patentability of this claim based on the additional limitations recited.

c. As per claims 3 and 16, applicant relies on the patentability of the claim from which this claim depends to traverse the rejection without prejudice to any further basis for patentability of this claim based on the additional limitations recited.

d. As per claims 4, 15, and 20, the Examiner asserts that Kelly discloses a first peripheral device communicatively coupled to the configurable link wherein the second level of access the peripheral device is capable of operating as the default bus master for the computer without assistance from the CPU, citing column 8, lines 32-50. The cited portion of Kelly discloses an IDLE mode in which the CPU-PCI bridge acts as a PCI master, drives the PCI bus, and prevents grant of the PCI bus. A mobile integrated system controller (MISC) interacts with the CPU-PCI bridge cause the bridge to release the PCI bus and allow the MISC to grant the PCI bus to other PCI masters. Applicant fails to understand the cited portion of Kelly disclosing anything about a peripheral device much less a peripheral device that is capable of operating as the default bus master as claimed. Applicant respectfully points out that a default bus master is more than a bus master in that the default bus master has the ability to select another device to become the bus master as discussed in the specification in the paragraph that begins on page 6, line 22. In the cited portion of Kelly the MISC, which is not a peripheral device, is the default bus master because it has the ability to grant the PCI bus to other PCI masters.

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- e. As per claims 5 and 19, the Examiner asserts that Kelly discloses a peripheral device coupled to the configurable link causes the configurable link to operate in the second level of access when the CPU is in a second power management state, citing column 5, lines 18-35. The cited portion of Kelly discloses a Mobile Super Input/Output (MSIO) device that provides a combination of standard ISA peripherals. Applicant does not understand anything in the cited portion to disclose a peripheral device that causes the configurable link to operate in the second level of access as claimed.
- f. As per claim 6 and 17, applicant relies on the patentability of the claim from which this claim depends to traverse the rejection without prejudice to any further basis for patentability of this claim based on the additional limitations recited.
- g. As per claims 7 and 18, applicant relies on the patentability of the claim from which this claim depends to traverse the rejection without prejudice to any further basis for patentability of this claim based on the additional limitations recited.
- h. As per claim 8, the Examiner asserts that Kelly discloses the transfer rate over the configurable link in the second level of access is different than in the first level of access, citing column 2, lines 15-25. The cited portion of Kelly discloses four power levels for a computer system. Applicant does not understand any of the power levels disclosed to include a transfer rate that varies based on two levels of access as claimed.
- i. As per claim 9, applicant relies on the patentability of the claim from which this claim depends to traverse the rejection without prejudice to any further basis for patentability of this claim based on the additional limitations recited.
- j. As per claim 10, applicant relies on the patentability of the claim from which this claim depends to traverse the rejection without prejudice to any further basis for patentability of this claim based on the additional limitations recited.
- k. As per claim 11, the Examiner asserts that Kelly discloses the configurable link enables the first peripheral device to manage the input/output hub to control communications to and from the first peripheral device in the second level of access, citing column 7, lines 39-51. The cited portion of Kelly discloses the CPU-PCI bridge transitioning between different power modes. Applicant fails to understand the cited portion of Kelly as disclosing a configurable link enables a first peripheral device to manage an input/output hub to control communications to and from the first peripheral device in a second level of access as claimed.
- l. As per claim 12, applicant relies on the patentability of the claim from which this claim depends to traverse the rejection without prejudice to any further basis for patentability of this claim based on the additional limitations recited.
- m. As per claim 13, the Examiner asserts that Kelly discloses the first peripheral device can communicate directly with the second peripheral device without assistance from the CPU in the second level of access, citing column 8, lines 32-67. The cited portion of Kelly discloses an IDLE mode in which the CPU-PCI bridge acts as a PCI master, drives the PCI bus, and

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prevents grant of the PCI bus. A mobile integrated system controller (MISC) interacts with the CPU-PCI bridge cause the bridge to release the PCI bus and allow the MISC to grant the PCI bus to other PCI masters. The CPU-PCI bridge drives the PCI bus to it pullup or pulldown conditions to minimize the power lost in the pullup or pulldown resistors. The Applicant fails to understand the cited portion of Kelly disclosing the first peripheral device can communicate directly with the second peripheral device without assistance from the CPU in the second level of access as claimed.

n. As per claim 21, the Examiner asserts that Kelly discloses each and every claimed limitation including a sub-system to configure a link coupling the input/output hub to a first peripheral device to allow the first peripheral device to manage data flow over the hub if the central processor is in a second power management state, citing column 4, lines 10-32. The cited portion of Kelly discloses the operation of a CPU-PCI bridge. Applicant does not understand Kelly to disclose that the CPU-PCI bridge can allow the first peripheral device to manage data flow over the hub if the central processor is in a second power management state as claimed.

o. As per claim 22, the Examiner asserts that Kelly discloses a sub-system to initiate a data transfer from the first peripheral device if the central processor is in the second power management state, citing column 7, lines 39-51. The cited portion of Kelly discloses the CPU-PCI bridge transitioning between different power modes. Applicant fails to understand the cited portion of Kelly as disclosing a sub-system to initiate a data transfer from the first peripheral device if the central processor is in the second power management state as claimed.

p. As per claim 23, the Examiner asserts that Kelly discloses a sub-system to buffer data at the first peripheral device if the central processor is in the second power management state, citing column 4, lines 10-32. The cited portion of Kelly discloses the operation of a CPU-PCI bridge. Applicant does not understand Kelly to disclose that the CPU-PCI bridge can buffer data at the first peripheral device if the central processor is in the second power management state as claimed.

q. As per claim 24, the Examiner asserts that Kelly discloses a sub-system to allow the first peripheral device to directly access and communicate with a second peripheral device without assistance from the central processor, citing column 8, lines 32-67. The cited portion of Kelly discloses an IDLE mode in which the CPU-PCI bridge acts as a PCI master, drives the PCI bus, and prevents grant of the PCI bus. A mobile integrated system controller (MISC) interacts with the CPU-PCI bridge cause the bridge to release the PCI bus and allow the MISC to grant the PCI bus to other PCI masters. The CPU-PCI bridge drives the PCI bus to it pullup or pulldown conditions to minimize the power lost in the pullup or pulldown resistors. The Applicant fails to understand the cited portion of Kelly disclosing a sub-system to allow the first peripheral device to directly access and communicate with a second peripheral device without assistance from the central processor as claimed.

r. As per claim 25, applicant relies on the patentability of the claim from which this claim depends to traverse the rejection without prejudice to any further basis for patentability of this claim based on the additional limitations recited.

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Applicant respectfully requests that the Examiner withdraw the rejection of claims 1-25 under 35 U.S.C. § 102(e) as being anticipated by Kelly.

Conclusion

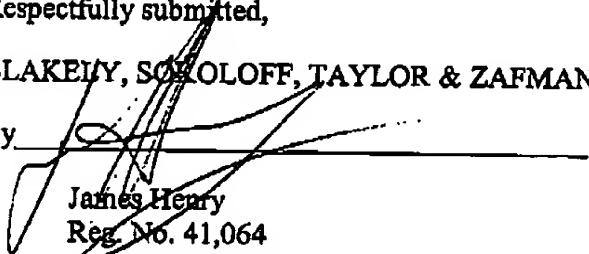
Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

BLAKELEY, SOLOLOFF, TAYLOR & ZAFMAN LLP

Dated: September 18, 2003

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